WHAT IS CLAIMED IS:

1. An electronic control unit comprising:

a plurality of CPUs;

a single non-volatile memory; and

communication ports connecting the CPUs and the non-volatile memory one another,

wherein a first one of the CPUs is programmed to check whether a second one of the CPUs is accessing the non-volatile memory before accessing the non-volatile memory, send to the second CPU a notification that the first CPU will access the non-volatile memory when a check result indicates that the second CPU is not accessing the non-volatile memory, and stops the notification to the second CPU after completing an access to the non-volatile memory.

2. The electronic control unit as in claim 1, wherein:

the CPUs are connected through the ports; and

the first CPU is programmed to set a signal level of the port to a level indicative of its accessing when starting to access the non-volatile memory.

3. The electronic control unit as in claim 1, wherein:

the CPUs are programmed to execute respective accessing to the non-volatile memory at different time points in initialization operations executed when a power supply to the CPUs is started.

4. The electronic control unit as in claim 3, wherein:

the first CPU is programmed to execute initialization operations of system registers thereof in divided manner thereby to differentiate the time points of the initialization operations from that of the second CPU.

5. The electronic control unit as in claim 3, wherein:

the CPUs are programmed to retrieve only specified high-priority data from the non-volatile memory in the respective initialization operations, and retrieves other low-priority data from the non-volatile memory only when required after completion of the initialization operations.

6. An electronic control unit comprising:

a plurality of CPUs;

a single non-volatile memory; and

communication ports connecting the CPUs and the non-volatile memory one another,

wherein a first one of the CPUs is programmed to transmit a data retrieving command, and the first CPU and the second CPU are programmed to receive at the same time same data from the non-volatile memory retrieved in response to the data retrieving command of the first CPU thereby to share the same retrieved data.

7. The electronic control unit as in claim 6, wherein the second CPU is programmed to receive the data retrieving command from the first CPU.

8. The electronic control unit as in claim 6, wherein:

the first CPU and the second CPU are programmed to be synchronized with each other and receive the same data from the non-volatile memory after being synchronized.

9. The electronic control unit as in claim 6, wherein:

the first CPU and the second CPU are programmed to retrieve respective individual data other than the same data separately from each other after receiving the same data.

10. The electronic control unit as in claim 6, wherein:

only the first CPU is programmed to transmit the data retrieving command as a master CPU, and the second CPU is programmed to receive the data retrieving command before receiving the same data from the non-volatile memory.

11. A data retrieving method in an electronic control unit having a first CPU, a second CPU and a single non-volatile memory, the method comprising the steps of:

generating a data retrieving command from the first CPU and notifying the second CPU that the first CPU transmits the data retrieving command;

retrieving data from the non-volatile memory in response to the data retrieving command; and

receiving the retrieved data by at least the first CPU directly from the non-volatile memory.

12. The method as in claim 11, further comprising the step of:

initializing a system register of the first CPU before generating the data retrieving command, the system register being associated with an access operation of the first CPU to the non-volatile memory; and

initializing other system registers of the first CPU after receiving the data from the non-volatile memory by the first CPU.

13. The method as in claim 12, further comprising the steps of:

initializing all system registers of the second CPU before generating a data retrieving command from the second CPU, so that data retrieving operations of the first CPU and the second CPU occurs at different time points.

14. The method as in claim 11, further comprising the step of:

generating a data retrieval command from the second CPU by checking that the first CPU is not accessing the non-volatile memory,

wherein the first CPU and the second CPU are capable of directly retrieving data from the non-volatile memory, respectively, independently of each other.

15. The method as in claim 14, wherein:

the first CPU and the second CPU retrieves only predetermined high-priority data from the non-volatile memory.

16. The method as in claim 11, wherein:

the data retrieving command is generated only by the first CPU; and

the retrieved data is received by both the first CPU and the second CPU at the same time.

17. The method as in claim 16, wherein:

the retrieved data is limited to data that are shared by both of the first CPU and the second CPU.

18. The method as in claim 17, further comprising the step of:

generating individual data retrieving commands from the first CPU and the second CPU to retrieve individual data other than the data to be shared from the non-volatile memory, respectively, after the data receiving step.

19. The method as in claim 16, further comprising the step of:

initializing system registers of the first CPU and the second CPU at the same time immediately after a start of power supply to the first CPU and the second CPU before generating the data retrieving command from the first CPU.

20. The method as in claim 19, further comprising the step of:

generating individual data retrieving commands from the first CPU and the second CPU to retrieve individual data other than the data to be shared from the non-volatile memory, respectively, after the data receiving step.